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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,080	01/09/2002	Richard D. Taylor	10010388	7522

7590 07/15/2004

AGILENT TECHNOLOGIES, INC.
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EXAMINER	
DUNCAN, MARC M	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/044,080	TAYLOR ET AL.
	Examiner	Art Unit
	Marc M Duncan	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1, 3-8 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadir et al.

Claims 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchiya.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Whittaker.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Hennessy.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Reams.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the combined parity bit memory, as outlined in claim 9, must be shown or the feature(s) canceled from the claim(s). Claim 9 states that a single parity bit is used for both the data store entry and its corresponding tag memory entry. The drawings show separate parity memories for the data store and the tag memory. No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if

only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadir et al.

Regarding claim 1:

Nadir teaches providing a read request to a system memory associated with the cache memory, the read request correlating to an entry in the tag memory and the data store in Fig. 4A "200" and col. 8 lines 62-65.

Nadir teaches checking the parity bit associated with the correlated entry in the tag memory and the parity bit associated with the correlated entry in the data store in Fig. 4A, Fig. 4B and col. 2 lines 65-67. The valid bit for the data store entry is equivalent to a parity bit because Nadir teaches that the validity of the data is determined using parity in col. 2 lines 65-67.

Nadir teaches if either act (a) or act (b) indicates an error in the corresponding correlated entry, declaring a miss Fig. 4A and Fig. 4B.

Regarding claim 3:

Nadir teaches invalidating the correlated entry in the data store if a miss is declared in act (c) in col. 9 lines 18-20 and lines 46-49.

Regarding claim 4:

Nadir teaches checking the parity bit associated with the correlated entry in the tag memory in Fig. 4B and col. 9 lines 42-45.

Nadir teaches if the parity bit associated with the correlated entry in the tag memory indicates no error: determining if the correlated entry in the tag memory indicates a hit in Fig. 4B.

Nadir teaches if there is a hit, checking the parity bit associated with the correlated entry in the data store in Fig. 4A and 4B and col. 5 line 67-col. 6 line 3.

Regarding claim 5:

Nadir teaches if the parity bit associated with the correlated entry in the data store indicates no error, retrieving the correlated entry from the data store in Fig. 4B "236." Continuing with normal processing after the hit is declared and all parity and

validity are determined inherently includes retrieving the correlated entry from the data store.

Regarding claim 6:

Nadir teaches wherein the retrieving the correlated entry from the data store act comprises retrieving the data line containing the correlated entry in Fig. 4B "236." Continuing with normal processing and retrieving the data inherently includes retrieving the data line containing the correlated entry.

Regarding claim 7:

Nadir teaches a data store in Fig. 1 "66."

Nadir teaches a tag memory in Fig. 1 "62."

Nadir teaches a parity bit memory configured to store a parity bit for each entry in the data store and for each entry in the tag memory in Fig. 1 "64." The valid bit for the data store entry is equivalent to a parity bit because Nadir teaches that the validity of the data is determined using parity in col. 2 lines 65-67.

Regarding claim 8:

Nadir teaches wherein each entry in the data store has a corresponding entry in the tag memory and wherein the parity bit stored for each entry in the data store is independent from the parity bit for the corresponding entry in the tag memory in Fig. 1 "76" and "78" and col. 3 lines 18-25.

Regarding claim 12:

Nadir teaches wherein the parity bit memory stores a single parity bit for each cache line in the data store in col. 5 lines 23-25.

Claims 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchiya.

Regarding claim 7:

Tsuchiya teaches a data store in the Abstract lines 3-4.

Tsuchiya teaches a tag memory in the Abstract lines 4-6.

Tsuchiya teaches a parity bit memory configured to store a parity bit for each entry in the data store and for each entry in the tag memory in the Abstract lines 8-14.

Regarding claim 9:

Tsuchiya teaches wherein each entry in the data store has a corresponding entry in the tag memory and wherein the parity bit memory is configured to store a single parity bit for each data store entry and its corresponding tag memory entry in the Abstract lines 4-14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Whittaker.

Regarding claim 2:

The teachings of Nadir are outlined above.

Nadir does not explicitly teach the cache being a second level cache. Nadir does, however, teach a cache memory.

Whittaker explicitly teaches a second level cache in Fig. 1.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the second level cache of Whittaker with the cache of Nadir.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the use of a second level cache reduces the miss penalty, which meets and expressed need of Nadir, namely, accessing the cache and retrieving data in the shortest possible time span.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Hennessy.

Regarding claim 10:

The teachings of Nadir are outlined above.

Nadir does not explicitly teach the cache being a write through cache. Nadir does, however, teach a cache memory.

Hennessy teaches a write through cache on page 607.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the write through cache of Hennessy with the cache of Nadir.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Hennessy teaches that write through caches provide for simpler and cheaper misses and that write through is easier to implement than write back.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadir in view of Reams.

Regarding claim 11:

The teachings of Nadir are outlined above.

Nadir does not explicitly teach the cache memory being a write back cache with a timeout flush. Nadir does, however, teach a cache memory.

Reams explicitly teaches a write back cache with a timeout flush in col. 1 lines 54-61.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the write back cache with a timeout flush of Reams with the cache memory of Nadir.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because a write back cache provides speed and efficiency because words can be written by the processor at the cache rate, rather than the slower memory rate. The timeout flush is performed to prevent accidental data loss and thereby increase reliability (see Reams col. 1 lines 54-61).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art not relied upon contains elements of the instant claims and/or represents a current state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 703-305-4622. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 703-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

SCOTT BADERMAN
PRIMARY EXAMINER